Summary
The course studies the most important techniques to exploit Instruction-Level Parallelism and discusses the relation with the critical phases of compilation. It also analyses emerging classes of processors for complex single-chip systems.

Content
Pushing processor performance to its limits:
- Principles of Instruction Level Parallelism (ILP).
- Register renaming techniques.
- Prediction and speculation.
- Simultaneous multithreading.
- VLIW and compiler techniques for ILP.
- Dynamic binary translation.

Embedded processors:
- Specificities over stand-alone processors.
- Overview of DSPs and related compilation challenges.
- Configurable and customisable processors.
- Basic notions of High-Level Synthesis.

Keywords

Learning Prerequisites
Required courses

- Architecture des ordinateurs.

Recommended courses

- Architecture des systèmes-on-chip.
Learning Outcomes
By the end of the course, the student must be able to:

• Design strategies to exploit instruction level parallelism in processors.
• Contrast static and dynamic techniques for instruction level parallelism.
• Design effective processor (micro-)architectures for which efficient compilers can be written.

Teaching methods
Courses, labs, and compulsory homeworks.

Assessment methods
Final oral exam.

Supervision
<table>
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<th>Office hours</th>
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<td>Assistants</td>
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Resources
Virtual desktop infrastructure (VDI)
No

Bibliography

Ressources en bibliothèque
• Computer Architecture / Hennessy

Moodle Link
• https://moodle.epfl.ch/course/view.php?id=15017