**Summary**

This course addresses the main aspects of the modeling of digital and mixed-signal hardware components and systems using the VHDL and the VHDL-AMS modeling languages.

**Content**

*Introduction*

System-on-chip (SoC) design issues. Design methodologies and design tasks. Notion of model. Modeling formalisms for digital and mixed-signal systems. Simulation and synthesis techniques.

*Modeling digital hardware components and systems*

Essential VHDL language elements and modeling concepts. VHDL synthesis subset. Modeling combinational and sequential/synchronous behaviors. Register-transfer level (RTL) modeling: modeling control (finite-state machines - FSM), modeling datapath, pipelining, generic RTL architecture (FSMD, algorithmic state machine (ASM)). From algorithm to digital hardware.

*Modeling analog and mixed-signal hardware components and systems*


**Keywords**

Digital hardware modeling. Analog and mixed-signal hardware modeling. VHDL. VHDL-AMS.

**Learning Prerequisites**

**Required courses**

Circuits and systems. Logic systems. Integrated digital circuits design. Analog circuits design.

**Important concepts to start the course**

Circuit and systems theory. Combinational and sequential logic components. Analog functional blocks (operational amplifier, filter, etc.).

**Learning Outcomes**

By the end of the course, the student must be able to:

- Describe available modeling formalisms for digital and mixed-signal hardware design.
- Produce quality and reusable VHDL and VHDL-AMS models.
- Choose proper modeling techniques.
- Assess / Evaluate the quality of a model w.r.t. its intended use.

**Teaching methods**
Lectures with integrated exercises.

**Expected student activities**

**Assessment methods**
Homework exercises. Midterm project. Final examination including a quiz and problems.

**Supervision**
Office hours No
Assistant Yes
Forum Yes

**Resources**
Virtual desktop infrastructure (VDI)
Yes

**Bibliography**

**Ressources en bibliothèque**
- *The System Designer’s Guide to VHDL-AMS* / Ashenden
- *VHDL-AMS and Verilog-AMS* / Pêcheux
- *Verification Methodology Manual for SystemVerilog* / Bergeron
- *VHDL for Logic Synthesis* / Rushton

**Notes/Handbook**
Course notes. VHDL and VHDL-AMS documentation. EDA tools user's guide.

**Websites**
- http://eda-tuts.epfl.ch/VHDLNutshell
- http://eda-tuts.epfl.ch/VHDLSimSyn

**Moodle Link**