Summary
In this project-based course, students collect hands-on experience with designing full-custom digital VLSI circuits in dynamic logic. They learn to carry out the design and optimization on transistor level, including logic and clock tree, the verification, and the layout.

Content

Keywords
VLSI, CMOS, transistor level, layout, adder, dynamic logic

Learning Prerequisites
Required courses
EE-429 Fundamentals of VLSI design
EE-490(b) Lab in EDA based design (or experience with CADENCE Virtuoso)

Learning Outcomes
By the end of the course, the student must be able to:
• Compose a transistor-level integrated circuit
• Analyze its performance
• Anticipate layout effects
• Design its layout

Teaching methods
Project based course with few lectures