EE-434 **Hardware systems modeling**

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Cursus	Sem.	Type
MNIS	MA3	Obl.

Language of teaching	English
Credits	2
Session	Winter
Semester	Fall
Exam	Written
Workload	60h
Weeks	14
Hours	**2 weekly**
Courses	2 weekly
Number of positions	

Summary

This course addresses the main aspects of the modeling of digital and mixed-signal hardware components and systems using the VHDL and the VHDL-AMS modeling languages.

Content

Introduction
System-on-chip (SoC) design issues. Design methodologies and design tasks. Notion of model. Modeling formalisms for digital and mixed-signal systems. Simulation and synthesis techniques.
Modeling digital hardware components and systems
Essential VHDL language elements and modeling concepts. VHDL synthesis subset. Modeling combinational and sequential/synchronous behaviors. Register-transfer level (RTL) modeling: modeling control (finite-state machines - FSM), modeling datapath, pipelining, generic RTL architecture (FSMD, algorithmic state machine (ASM)). From algorithm to digital hardware.
Modeling analog and mixed-signal hardware components and systems
Essential VHDL-AMS language elements and modeling concepts. Modeling electrical primitives, operational amplifier, filters, A/D and D/A interfaces, A/D and D/A converters.

Keywords

Digital hardware modeling. Analog and mixed-signal hardware modeling. VHDL. VHDL-AMS.

Learning Prerequisites

Required courses

Circuits and systems. Logic systems. Integrated digital circuits design. Analog circuits design.

Important concepts to start the course

Circuit and systems theory. Combinational and sequential logic components. Analog functional blocks (operational amplifier, filter, etc.).

Learning Outcomes

By the end of the course, the student must be able to:

- Describe available modeling formalisms for digital and mixed-signal hardware design.
- Produce quality and reusable VHDL and VHDL-AMS models.
- Choose proper modeling techniques.
- Assess / Evaluate the quality of a model w.r.t. its intended use.

Teaching methods

Lectures with integrated exercises.

Expected student activities

Attending lectures. Completing exercises. Using state-of-the-art electronic design automation (EDA) tools.

Assessment methods

Homework exercises. Midterm project. Final examination including a quiz and problems.

Supervision

Office hours	No
Assistants	Yes
Forum	Yes

Resources

Bibliography

P. Ashenden, G. Peterson, and D. Teegarden, *The System Designer's Guide to VHDL-AMS*, Morgan Kaufmann, 2002.
J. Bergeron, et al., *Verification Methodology Manual for SystemVerilog*, Springer, 2005.
P.P. Chu, *RTL Hardware Design Using VHDL: Coding for Efficiency, Portability, and Scalability*, Wiley-Interscience, 2006.
F. Pêcheux, C. Lallement, and A. Vachoux, "*VHDL-AMS and Verilog-AMS as alternative hardware description languages for efficient modeling of multidiscipline systems*," IEEE Trans. on Computer-Aided Design of Integrated Circuits and Systems, vol. 24, pp. 204-225, 2005.
A. Rushton, *VHDL for Logic Synthesis*, 3rd ed.: Wiley, 2011.

Ressources en bibliothèque

- The System Designer's Guide to VHDL-AMS / Ashenden
- VHDL for Logic Synthesis / Rushton
- Verification Methodology Manual for SystemVerilog / Bergeron
- VHDL-AMS and Verilog-AMS / Pêcheux

Notes/Handbook

Course notes. VHDL and VHDL-AMS documentation. EDA tools user's guide.

Websites

- http://www.doulos.com/knowhow/vhdl_designers_guide
- http://esd.cs.ucr.edu/labs/tutorial
- http://en.wikipedia.org/wiki/VHDL-AMS

Moodle Link

- http://moodle.epfl.ch/course/view.php?id=13977