EE-432 **Hardware systems modeling I**

Vachoux Alain

Cursus	Sem.	Type
Electrical and Electronical Engineering	MA1, MA3	Opt.
Mineur STAS Chine	H	Opt.

Language of teaching	English
Credits	2
Session	Winter
Semester	Fall
Exam	Written
Workload	60h
Weeks	14
Hours	**2 weekly**
Courses	2 weekly
Number of positions	

Summary

Creation and use of models in digital hardware design from the RTL design with the VHDL language to the more abstract system level as required for designing modern systems-on-chip. The SystemVerilog and SystemC languages and the principles of functional verification will be introduced.

Content

Introduction
System-on-chip (SoC) design issues. Design methodologies and design tasks. Notion of model. Hardware description and verification languages at RTL and system level.
Digital hardware modeling at RTL and system level
Review of essential modeling concepts in RTL design using VHDL. Discrete-event (DE) modeling. Untimed modeling (algorithmic, functional). Transaction-level modeling (TLM). Dataflow (DF) modeling. Modeling using SystemVerilog and SystemC.
Functional verification of systems-on-chip
Fundamental elements of the functional verification for SoCs: challenges of the verification of complex SoCs, verification methodologies, definition and use of a verification plan, architecture and elements of a layered verification environment. Use of Open Source VHDL Verification Methodology (OSVVM) for building an efficient and scalable functional verification environment.

Keywords

Hardware description and verification language, model of computation, functional verification, VHDL, SystemVerilog, SystemC.

Learning Prerequisites

Required courses

Logic systems (CS-171). Digital Systems Design (EE-334).

Recommended courses

Lab in digital systems design (EE-397).

Important concepts to start the course

Combinational and sequential components in digital electronic systems. RTL design (control and datapath processing). Use of VHDL for synthesis.

Learning Outcomes

By the end of the course, the student must be able to:

- Describe available modeling formalisms for digital hardware system design.
- Compare the proper use of available modeling formalisms.
- Use VHDL, SystemVerilog and SystemC for developing models at various levels of abstraction.
- Exploit proper modeling techniques.
- Develop reusable models.
- Construct a basic functional verification environment.

Teaching methods

Lectures with integrated exercises.

Expected student activities

Attending lectures. Completing exercises. Using state-of-the-art electronic design automation (EDA) tools.

Assessment methods

Homework exercises. Midterm project. Final examination including a quiz and problems.

Supervision

Office hours	No
Assistants	Yes
Forum	Yes
Others	Individual feedback comments on delivered work in the Moodle page of the course.

Resources

Bibliography

A. Jantsch, *Modeling Embedded Systems and SOC's*, Morgan Kaufmann (Elsevier), 2004.
P.P. Chu, *RTL Hardware Design Using VHDL: Coding for Efficiency, Portability, and Scalability*, Wiley-Interscience, 2006.
T. Grötker, et al., *System Design with SystemC*, Springer, 2002.
C. Spear, G. Tumbush, *SystemVerilog for Verification - A Guide to Learning the Testbench Language Features*, Springer, 3rd ed., 2012.

Ressources en bibliothèque

- SystemVerilog for Verification / Spear
- Modeling Embedded Systems and SOC's / Jantsch
- RTL Hardware Design Using VHDL / Chu
- System Design with SystemC / Grötker

Notes/Handbook

Course notes. VHDL/SystemVerilog/SystemC in a nutshell. EDA tool user's guide.

Websites

- http://www.doulos.com/knowhow/vhdl_designers_guide
- http://www.doulos.com/knowhow/sysverilog
- http://www.doulos.com/knowhow/systemc

Moodle Link

- http://moodle.epfl.ch/course/view.php?id=40

Prerequisite for

Hardware systems modeling II (EE-433). VLSI design II (EE-431).