

EE-606

**Nanocomputing: Devices, Circuits and Architectures (2019)**

Carrara Sandro, Demarchi Danilo, Graziano Mariagrazia, Piccinini Gianluca

| Cursus                 | Sem. | Type |                            |                |
|------------------------|------|------|----------------------------|----------------|
| Electrical Engineering |      | Obl. | Language of teaching       | English        |
|                        |      |      | Credits                    | 1              |
|                        |      |      | Session                    |                |
|                        |      |      | Exam                       | Project report |
|                        |      |      | Workload                   | 30h            |
|                        |      |      | <b>Hours</b>               | <b>18</b>      |
|                        |      |      | Courses                    | 18             |
|                        |      |      | <b>Number of positions</b> | <b>20</b>      |

**Frequency**

Every year

**Remark**

Every year. Next time: Spring 2018

**Summary**

This course aims at giving the student a detailed overview of the computation circuits and systems for computations that are expected to become the main actor in the forthcoming scenario, going beyond the ultra-scaled CMOS technologies and focusing the attention on the emerging technologies.

**Content**

The student will have a good overview of the novel solutions offered by the nanotechnologies. He will have an exhaustive coverage starting from the technology, passing to the devices up to the architectures. One of the training goals of the course is to give to the student a scenario form which to choose a specific topic of particular interest, that will be studied and developed for the preparation of the final Project Report.

## 1. State of the art: nanocomputing in ULTRA scaled CMOS:

- CMOS scaling trends at device levels: scaling, leakage, double-gate transistors, FinFET, etc.
- Circuit and architectural techniques: dark silicon, dynamic voltage scaling, subthreshold computation, etc.

## 2. Field coupled nanocomputing (FCN):

- a new principle: computing through field coupling and not through transport
- devices: quantum dot cellular automata (QCA), nano magnetic logic (NML), molecular QCA, silicon based QCA; discussions on technology, behavior, models, energy consumption, speed, area
- interconnections: magnetic domain walls, spin waves, molecular wires
- designing a FCN circuit: a new design paradigm toward intrinsic pipelining
- circuits and architectures based on FCN structures: synchronous, asynchronous, null-convention logic; how to solve feedback problems; cut set retiming; solutions based on systolic arrays and interleaving

## 3. Nanoarray nanocomputing based on nanowires:

- devices: Gate-All-Around transistors, Ambipolar transistors (silicon based, zinc-oxide, carbon nanotubes, ...)

- circuits: nano-PLA, NanoASIC, reconfigurable nanoFPGA
- architectures: sea of nanoarrays for massive computation and "embarrassingly parallel" elaboration

4. Logic in memory:

- Devices: resistive memories, memristors, nanomagnets and magnetic memories
- Circuits: logic embedded in memory, communications and protocols
- Architectures: caches to the limit, use hic what you need nunc, search nearby what you need later

5. Alternative nanocomputing devices and architectures:

- Molecular computing, Biological computing, Spintronic computing, Cellular automata, Quantum computing

**Keywords**

Nanocomputing; Beyond CMOS; Quantum Cellular Automata (QCA); Quantum Computing.

**Learning Prerequisites**

**Required courses**

Basic courses in silicon technologies and CMOS architectures.