MICRO-708

Nano CMOS Devices & Technologies for Tera-Bit Circuits and Systems

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Cursus	Sem.	Type
Electrical Engineering		Obl.
Microsystems and Microelectronics		Obl.

Language of teaching	English
Credits	1
Session	
Exam	Project report
Workload	30h
Hours	**15**
Courses	15
Number of positions	**20**

Frequency

Every 2 years

Remark

July 2 to 4, 2018. CANCELLED

Summary

The "Nano CMOS Devices & Technologies for Tera-Bit Circuits and Systems" course delivers what a CMOS engineer should really know of technology, devices and circuits.

Content

1. presentation and discussion of technological, physical and circuit/system limitations of the actual CMOS (MOSFET & interconnect scaling, multicore processing, SRAM variability problems, power dissipation, etc.)
2. physical understanding/simple models of these limitations - their analysis and hints on possible improvements - confrontation with actual industrial practice
3. qualitative and quantitative analysis of advanced Bulk technology modules aimed at curing the actual CMOS - HK dielectrics, metal gate, spike annealing, impact on SRAM, on leakage, on power dissipation, etc.
4. analysis of nano-technologies /device architectures aimed at removing the limitations of the actual CMOS - breakthrough solutions for Tera-Bit circuits - devices down to 5-10nm - Double Gate, FDSOI - multiple core processing, design and layout solutions aiming at improvement in SRAM variability, power dissipation etc.
5. Circuit implications (Inverter, Ring Oscillator) and predictions on CMOS Roadmap - what future CMOS will be able to do and what it will not. Acquisition and familiarization with MASTAR - the tool serving for conception of the ITRS CMOS Roadmaps - explanation of the examination project - Design your own CMOS Roadmap !

Keywords

CMOS, Roadmap, ITRS, Tera-Bit, Low Power, Mobile, Multimedia, layout, power management, MOSFET, interconnects, fluctuations, short-channel effects (SCE), quantum effects, SRAM, variability, power dissipation, gate leakage, drain-induced barrier lowering (DIBL), mobility, H-K dielectrics, metallic gate, ultra-shallow junctions, Schottky junctions, strained Silicon, SiGe, Ge and GaAs, rotated substrates, FD SOI, Silicon On Nothing, Double Gate, FinFET devices, 10nm devices, Cross-bar, 3D integration, Beyond CMOS, Nano-technologies.

Learning Prerequisites

Recommended courses

Basic knowledge of electrostatics and materials (potential, field, electron flow, diffusion), of MOS transistor (field effect, depletion, inversion), and of basic logic gates (Inverter, NAND, NOR, ring oscillator)