

# EE-606 Nanocomputing: Devices, Circuits and Architectures (2019)

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Cursus	Sem.	Type
Electrical Engineering		Obl.

Language of teaching	English
Credits	1
Session	
Exam	Project report
Workload	30h
Hours	18
Courses	18
Number of	20
positions	

### Frequency

Every year

## Remark

Every year. Next time: Spring 2019

#### **Summary**

This course aims at giving the student a detailed overview of the computation circuits and systems for computations that are expected to become the main actor in the forthcoming scenario, going beyond the ultra-scaled CMOS technologies and focusing the attention on the emerging technologies.

#### Content

The student will have a good overview of the novel solutions offered by the nanotechnologies. He will have an exaustive coverage starting from the technology, passing to the devices up to the architectures. One of the training goals of the course is to give to the student a scenario form which to choose a specific topic of particular interest, that will be studied and developed for the preparation of the final Project Report.

- 1. State of the art: nanocomputing in ULTRA scaled CMOS:
- CMOS scaling trends at device levels: scaling, leakage, double-gate transistors, FinFET, etc.
- Circuit and architectural techniques: dark silicon, dynamic voltage scaling, subthreshold computation, etc.
- 2. Field coupled nanocomputing (FCN):
  - a new principle: computing through field coupling and not through transport
  - devices: quantum dot cellular automata (QCA), nano magnetic logic (NML), molecular QCA, silicon basedQCA; discussions on technology, behavior, models, energyconsumption, speed, area
  - interconnections: magnetic domain walls, spin waves, molecular wires
  - designing a FCN circuit: a new design paradigm toward intrinsic pipelining
  - circuits and architectures based on FCN structures: syncrhonous, asynchronous, null-convention logic; howto solve feedback problems; cut set retiming; solutions based on systolic arrays and interleaving
- 3. Nanoarray nanocomputing based on nanowires:
  - devices: Gate-All-Around transistors, Ambipolar transistors (silicon based, zinc-oxide, carbon nanotubes, ...)



- circuits: nano-PLA, NanoASIC, reconfigurable nanoFPGA
- architectures: sea of nanoarrays for massive computation and "embarassingly parallel" elaboration
- 4. Logic in memory:
  - Devices: resistive memories, memristors, nanomagnets and magnetic memories
  - Circuits: logic embedded in memory, communications and protocols
  - Architectures: caches to the limit, use hic what you need nunc, search nearby what you need later
- 5. Alternative nanocomputing devices and architectures:
  - Molecular computing, Biological computing, Spintronic computing, Cellular automata, Quantum computing

### Keywords

Nanocomputing; Beyond CMOS; Quantum Cellular Automata (QCA); Quantum Computing.

## **Learning Prerequisites**

## **Required courses**

Basic courses in silicon technologies and CMOS architectures.

## **Assessment methods**

Project report.