EE-535

Nanoelectronics

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Cursus	Sem.	Type
Electrical and Electronical Engineering	MA1, MA3	Opt.
MNIS	MA3	Obl.

Language of teaching	English
Credits	2
Session	Winter
Semester	Fall
Exam	Written
Workload	60h
Weeks	14
Hours	**2 weekly**
Courses	2 weekly
Number of positions	

Summary

This lecture overviews and discusses the last trends in the technology and principles of nanoelectronic devices for more aggressive scaling, better performances, added functionalities and lower energy per function. The opportunities of these advances compared to industrial roadmaps are analized.

Content

(1) Ultimate CMOS technologies and their showstoppers

(2) Phenomena specific to deep submicron devices: non-stationary phenomena (velocity overshoot), ballistic transport, quantum effects, atomic scale parameter fluctuation (fluctuation of number of dopants, interface roughness).

(3) Innovative device architectures (Double-gate MOS transistor - DGMOS, dynamic threshold MOS transistor - DTMOS, gate-all-around transistor - GAA, vertical MOS transistors)

(4) Nano-scale and quantum devices: Single Electron Transistor (SET), quantum wires, few-electron memories, etc.

(5) Steep slope switches: Tunnel FEts, NEM switch and Negative Capacitance switch.

(6) Charge-based circuit architectures: quantum dot cellular automata (QCA)

(7) Carbon Nanotubes: technology, devices and circuits

(8) Spintronics

Learning Prerequisites

Recommended courses

Basic electronics

Teaching methods

Ex cathedra

Assessment methods

Written