EPFL

EE-520	**Low-power analog IC design**
	Enz Christian

Cursus	Sem.	Type
Data and Internet of Things minor	H	Opt.
Electrical and Electronical Engineering	MA1, MA3	Opt.
MNIS	MA3	Opt.
Microtechnics	MA1, MA3	Opt.

Language of teaching	English
Credits	2
Session	Winter
Semester	Fall
Exam	Written
Workload	60h
Weeks	14
Hours	**2 weekly**
Courses	2 weekly
Number of positions	

Summary

This course presents the design of low-power analog CMOS integrated circuits. The techniques are based on the concept of inversion coefficient that can be used as the main design parameter for the optimization of figures-of-merit applied to circuits including amplifiers, filters and oscillators.

Content

1. Introduction
2. CMOS Technology Scaling
3. Modeling of the MOS Transistor for Low-power Design
4. The Concept of Inversion Coefficient and Gm/ID Design Methodology
5. Optimization of Basic Figures-of-merit
6. Amplifiers (OTAs and OPAMPs)
7. Offset and 1/f Noise Reduction Techniques
8. Continuous-time (CT) Filters Design
9. Switched-capacitors (SC) Filters Design
10. Oscillators

Keywords

Low-power, Analog, CMOS, Low-noise

Learning Prerequisites

Required courses

- Basic circuit theory course.
- Basic analog circuit design course.
- Semiconductor device modeling course.
- Basic analog integrated circuits design course.

Recommended courses

- Analog filter design course.
- Course on random processes and noise in devices and circuits.

Learning Outcomes

By the end of the course, the student must be able to:

- Design low-power analog circuits
- Optimize power and other figures-of-meritt
- Analyze simple analog circuits
- Dimension transistors of a given circuit to achieve desired specifications
- Verify performace by simulations
- Formalize analog circuit design procedure
- Select appropriately the correct design parameters
- Represent the trade-offs in an optimal way
- Choose the correct operating point

Transversal skills

- Use a work methodology appropriate to the task.
- Continue to work through difficulties or initial failure to find optimal solutions.
- Use both general and domain specific IT resources and tools

Teaching methods

Two hours weekly lecture

Expected student activities

In addition to studying the lecture notes the student will have to do some home work

Assessment methods

Written exam.

Resources

Bibliography

Device modeling:
[1] C. C. Enz and E. A. Vittoz, Charge-based MOS Transistor Modeling, Wiley, 2006.
[2] Y. Tsividis and C. Mc Andrew, Operation and Modeling of the MOS Transistor, 3rd ed., Oxford University Press, 2001.
CMOS IC design:
[3] T. C. Carusone, D. A. Johns, K. W. Martin, Analog Integrated Circuit Design, 2nd edition, Wiley, 2012.
[4] B. Razavi, Design of Analog CMOS Integrated Circuits, 2nd ed., Mc Graw Hill, 2017.
[5] W. Sansen, Analog Design Essentials, Springer, 2013.
[6] A. Sedra, K. Smith, Microelectronic Circuits, 7th edition, Oxford University Press, 2015.
[7] P. R. Gray, P. J. Hurst, S. H. Lewis and R. G. Meyer, Analysis and Design of Analog Integrated Circuits, 5th ed., Wiley, 2009.
Gm/ID design methodology:
[8] David Binkley, Tradeoffs and Optimization in Analog CMOS Design, Wiley, 2008.
[9] P. Jespers, B. Murmann, Systematic Design of Analog CMOS Circuits, Cambridge, 2017.
[10] P. Jespers, The Gm over ID Methodology, Springer, 2010.

Ressources en bibliothèque

- Charge-based MOS Transistor Modeling / Enz
- Analog Design Essentials / Sansen
- Analysis and Design of Analog Integrated Circuits / Gray
- Microelectronic Circuits / Sedra
- Tradeoffs and Optimization in Analog CMOS Design / Binkley

- Operation and Modeling of the MOS Transistor / Tsividis
- Design of Analog CMOS Integrated Circuits / Razavi
- The Gm over ID Methodology / Jespers
- Analog Integrated Circuit Design / Carusone
- Systematic Design of Analog CMOS Circuits / Jespers

Notes/Handbook
Slides will be provided on the moodle site.