EE-424

Fundamentals of analog VLSI design

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Cursus	Sem.	Type
Data and Internet of Things minor	H	Opt.
Electrical and Electronical Engineering	MA1, MA3	Obl.
Electrical and electronic engineering minor	H	Opt.
Microtechnics	MA1, MA3	Opt.

Language of teaching	English
Credits	4
Session	Winter
Semester	Fall
Exam	Written
Workload	120h
Weeks	14
Hours	**4 weekly**
Courses	2 weekly
Exercises	2 weekly
Number of positions	

Summary

This course presents the systematic design of low-power analog CMOS integrated circuits based on the concept of inversion coefficient and on the sEKV MOSFET model. It covers device modeling, basic building blocks to more advanced circuits like amplifiers and switched-capacitor circuits.

Content

1) Introduction
2) Technology roadmap
3) Modeling of the MOS transistor for low-power design
4) The concept of inversion coefficient and Gm/ID design methodology
5) Optimization using basic figures-of-merit
6) Amplifiers (OTAs and OPAMPs)
7) Offset and 1/f noise reduction techniques
8) Continuous-time (CT) filters
9) Switched-capacitors (SC) filters
10) Oscillators

Keywords

Analog, Circuits, CMOS, Low-power, EKV

Learning Prerequisites

Required courses

Basic analog circuits (discrete)
Basic circuit analysis
Semiconductor device modeling

Recommended courses

Noise in circuits and systems
EDA

Important concepts to start the course

Analysis of linear circuits

Laplace transform and frequency response
Small-signal circuit concept

Learning Outcomes

By the end of the course, the student must be able to:

- Design analog integrated circuits
- Verify the correct operation by circuit simulation
- Analyze analog circuits including the noise
- Optimize the circuit for achieving given specifications
- Investigate various circuit options
- Present the selected options
- Justify his design choices
- Report on the final design

Transversal skills

- Use a work methodology appropriate to the task.
- Use both general and domain specific IT resources and tools
- Demonstrate the capacity for critical thinking

Teaching methods

The 2 hours lectures are combined with a 1 hour exercise session and a 1 hour computer simulation session. Often the exercise and the computer simulation will be interweaved. Computer tools will be used for the analysis and the design (typically Jupyter Notebooks) and verification will be done with a circuit simulator (such as ngspice).

Expected student activities

The student will do homework to prepare and validate the work done during the exercise and simulation sessions.

Assessment methods

The exam is an MCQ which is ran on Moodle. It is open-book and requires a laptop to access Moodle.
There is no mid-term exam.

Resources

Bibliography

The lecture is based on the following textbooks:
Device modeling:
[1] C. C. Enz and E. A. Vittoz, *Charge-based MOS Transistor Modeling*, Wiley, 2006.
[2] Y. Tsividis and C. Mc Andrew, *Operation and Modeling of the MOS Transistor*, 3rd ed., Oxford University Press, 2001.
CMOS IC design:
[3] T. C. Carusone, D. A. Johns, K. W. Martin, *Analog Integrated Circuit Design*, 2nd edition, Wiley, 2012.
[4] B. Razavi, *Design of Analog CMOS Integrated Circuits*, 2nd ed., Mc Graw Hill, 2017.
[5] W. Sansen, *Analog Design Essentials*, Springer, 2013.
[6] A. Sedra, K. Smith, *Microelectronic Circuits*, 7th edition, Oxford University Press, 2015.
[7] P. R. Gray, P. J. Hurst, S. H. Lewis and R. G. Meyer, *Analysis and Design of Analog Integrated Circuits*, 5th ed., Wiley, 2009.

Gm/ID design methodology:
[8] David Binkley, *Tradeoffs and Optimization in Analog CMOS Design*, Wiley, 2008.
[9] P. Jespers, B. Murmann, *Systematic Design of Analog CMOS Circuits*, Cambridge, 2017.
[10] P. Jespers, *The Gm over ID Methodology*, Springer, 2010.

Ressources en bibliothèque

- Find the references at the Library

Websites

- https://github.com/chrisenz/EPFL-EE-424
- https://github.com/chrisenz/sEKV-Design-in-IHP-SG13G2

Moodle Link

- https://go.epfl.ch/EE-424