

EE-334

**Digital systems design**

Burg Andreas Peter

Cursus	Sem.	Type
Electrical and Electronical Engineering	BA5	Obl.
HES - EL	H	Obl.
MNIS	MA3	Obl.

Language of teaching	English
Credits	4
Session	Winter
Semester	Fall
Exam	Written
Workload	120h
Weeks	14
<b>Hours</b>	<b>4 weekly</b>
Courses	2 weekly
Exercises	2 weekly
<b>Number of positions</b>	

**Summary**

Students will acquire basic knowledge about methodologies and tools for the design, optimization, and verification of custom digital systems/hardware. They learn how to design synchronous digital circuits on register transfer level, analyse their timing and implement them in VHDL and on FPGAs.

**Content****Digital systems**

Views and abstractions in digital hardware systems, formalisms for system description.

**Register-transfer-level (RTL) design**

Methodology translating a high-level (algorithmic) system description into control and datapath structures, foundations of synchronous digital design, timing and timing constraints, basic architectural transformations, FPGA basics.

**VHDL**

VHDL language basics and event-driven simulation, VHDL RTL design, synthesis and verification.

**Keywords**

Digital hardware component/system, register-transfer-level design, RTL, VHDL, synthesis, verification, FPGA.

**Learning Prerequisites****Required courses**

Logic systems (CS-171). Microcontrollers and digital systems design (EE-208).

**Important concepts to start the course**

Combinational and sequential logic components. Basic computing unit architecture.

**Learning Outcomes**

By the end of the course, the student must be able to:

- Explain the principles and rules for safe and robust synchronous design.
- Optimize datapaths for timing and area.
- Develop state machines and control structures for digital circuits.
- Translate a register-transfer-level design into a synthesizable VHDL model.
- Synthesize datapaths and control from a high-level specification to FPGA.
- Test the correct functionality of RTL and synthesized VHDL models.

**Teaching methods**

Ex-cathedra with exercises in groups and small projects using FPGA design tools and platforms.

### Expected student activities

Attending lectures. Completing exercises and projects. Use FPGA design tools.

### Assessment methods

Graded Homework and Final Exam

### Resources

#### Bibliography

R. Airiau, et al., *VHDL: Langage, modélisation, synthèse*, Presses Polytechniques et Universitaires Romandes, 2003.

H. Kaeslin, *Digital Integrated Circuit Design: From VLSI Architectures to CMOS Fabrication*, Cambridge Univ. Press, 2008.

A. Rushton, *VHDL for Logic Synthesis*, 3rd ed.: Wiley, 2011.

#### Ressources en bibliothèque

- [Find the references at the Library](#)

#### Notes/Handbook

Lecture handouts and notes. VHDL syntax summary. FPGA design tools user's guides.

#### Moodle Link

- <https://go.epfl.ch/EE-334>

### Prerequisite for

TL in Micro and nanoelectronics, TP in micro-nano, EDA-Based Design, Fundamentals of VLSI