

EE-490(b)

Lab in advanced VLSI design

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Cursus	Sem.	Type
Electrical and Electronical Engineering	MA2, MA4	Opt.
Electrical and electronic engineering minor	E	Opt.

Language of teaching	English
Credits	4
Withdrawal Session	Unauthorized Summer
Semester Exam	Spring During the semester
Workload	120h
Weeks	14
Hours	4 weekly
TP	4 weekly

Number of positions

Il n'est pas autorisé de se retirer de cette matière après le délai d'inscription.

Summary

this class covers advanced VLSI design techniques. top-down full custom circuit design.

Content

Schematic edition. Advanced simulation techniques for CMOS circuits. Complex parametric analysis and multiparametric optimization. Floorplanning. Clock distribution network. Physical design and layout. Optimization for parasitics mitigation. Post layout analysis and optimization. defend their design choices in a presentation.

Keywords

VLSI
circuit design
CMOS

Learning Prerequisites**Recommended courses**

Fundamentals of VLSI, EE-429

Important concepts to start the course

CMOS schematic and layout edition with Cadence virtuoso
Simulation of circuits using cadence ADE

Learning Outcomes

By the end of the course, the student must be able to:

- Justify their choices
- Optimize a circuit
- Plan their time properly
- Implement their plan

- Explore various possibilities
- Assemble a complex design
- Estimate the remaining effort
- Decide what to do

Transversal skills

- Plan and carry out activities in a way which makes optimal use of available time and other resources.
- Continue to work through difficulties or initial failure to find optimal solutions.
- Make an oral presentation.

Teaching methods

lecture
guided labs
project

Expected student activities

attendance at lectures
doing a project
preparing an oral presentation

Supervision

Office hours	Yes
Assistants	Yes
Forum	Yes

Resources

Virtual desktop infrastructure (VDI)

Yes

Moodle Link

- https://go.epfl.ch/EE-490_b