MICRO-710

PLLs and clock & data recovery

Kayal Maher

Cursus	Sem.	Type
Electrical Engineering		Opt.
Microsystems and Microelectronics		Opt.

Language of teaching	English
Credits	2
Session	
Exam	Written & Oral
Workload	60h
Hours	**28**
Lecture	28
Number of positions	

Remark

Cours supprimé du plan d'études EDMI et EDEE

Summary

The course is covering following aspects: Fundamentals of Analog PLLs, Interference Effects, Deadzone and Phase Noise, VCO Design, All-Digital PLL Architecture and Implementation, Digitally-Controlled Oscillator, Time-to-Digital Converter, RC-Oscillators, Designing XTAL and MEMS Oscillator.

Content

Day 1:
- Fundamentals of Analog PLLs
- Interference Effects in PLLs
- Spiral Inductor Interference, Deadzone and Phase Noise

Day 2:
- VCO Design
- Jitter and Phase Noise in PLLs

Day 3:
- All-Digital PLL Architecture and Implementation
- Digitally-Controlled Oscillator (DCO)
- Time-to-Digital Converter (TDC)

Day 4:
- Oscillator Basics: Feedback and Power Consumption
- RC-Oscillators
- Designing XTAL and MEMS Oscillator from MHz to GHz
- Low Phase Noise and Low Jitter 0.1-10GHz VCO

Day 5:
- Fractional-N PLLs for Frequency Synthesis
- FDC-Based Digital PLLs

Keywords

Clock Recovery, PLL, VCO Circuits, Oscillators, Transceivers

Learning Prerequisites

Recommended courses

Analog IC Design

Resources

Ressources en bibliothèque

- Analog-to-Digital Conversion / Pelgrom
- Structured Analog CMOS Design / Kayal
- Understanding delta-sigma data converters / Schreier
- Understanding Delta-Sigma Data Converters / Pavan
- Methodology for the Digital Calibration of Analog Circuits & Systems / Kayal
- All-Digital Frequency Synthesizer in Deep-Submicron CMOS / Staszewski
- Charge-Based MOS Transistor Modeling: The EKV Model for Low-Power and RF IC Design / Enz
- Analog Design Essentials / Sansen
- RF analog impairments modeling for communication systems simulation : application to OFDM-based transceivers / Smaini