MICRO-727

# Beyond CMOS devices and advanced computing architectures

Invited lecturers (see below), Ionescu Mihai Adrian, Moselund Kirsten Emilie

| Cursus | Sem. | Type |
|---|---|---|
| Microsystems and Microelectronics | | Opt. |

| | |
|---|---|
| Language of teaching | English |
| Credits | 1 |
| Session | |
| Exam | Written |
| Workload | 30h |
| **Hours** | **14** |
| Courses | 14 |
| **Number of positions** | |

## Frequency

Every 2 years

## Remark

November 10 to 12, 2026

## Summary

This course will discuss trends in nanoelectronics for transistor scaling, better performances and lower energy per function. It covers emerging architectures such as in memory computing and transistor applications for high power, high frequency or cryogenic operation.

## Content

The course consists of 7 lectures on hot topics on beyond CMOS and advanced architectures which will be given by different specialists in the field:

***Prof. Kirsten E. Moselund, EPFL & PSI: Moore's law & scaling, advanced CMOS architectures***

*Moore's law has survived for more than half a century, together with Dennard scaling it enabled the IC revolution which went from a few thousand to billions of transistors on a chip. Whereas we continue to increase the numbers of transistors and complexity of modern computer chip, the laws of scaling have fundamentally changed. In this lecture we will cover the evolution in transistor architecture from planar over FinFET to today's nanosheet devices and the C-FETs of future scaled nodes. We will focus on the material breakthroughs which made this possible and discuss bottle necks of future device sacling.*

***Dr. Cezar Zota,* IBM Research*: "Beyond the device level: Thermal, interconnect and integration challenges in CMOS"***

Description: *As transistor counts have reached billions on a single chip, further scaling now faces several inter-related challenges at higher levels of the chip hierarchy, which will be examined in this lecture. While CMOS transistors improve when scaled down in size, in contrast, the nanoscale metal lines that connect those devices together degrade due to confined surface scattering. The solution is to go beyond the conventional metals used today, mainly copper, towards materials resilient to scattering, such as 2D materials and exotic topological conductors. In tandem, new integration approaches are being developed to relax interconnect density, such as back-side power delivery, where transistors are contacted from both top and bottom. However, this requires the removal of the substrate, which, in turn, leads to excessive heating of the chip and hot spot formation, reducing performance and degrading lifetime. Innovative solutions to characterize and mitigate thermal effects, such as diamond-based thermal scaffolding, will be required to enable future ultra-high-performance chips.*

**Dr. Ghazi Sarwat Syed, IBM Research: "Computing Where the Data Lives: An Introduction to In-Memory Computing"**

*A central challenge in modern computing is the processor-memory bottleneck: the repeated shuttling of data between memory and processors makes computation slow and energy-in efficient. In-memory computing (IMC) tackles this by bringing computation directly into the memory unit, exploiting the intrinsic physical properties and array-level organization of memory devices rather than moving data to where the processing happens. This lecture unpacks the core principles of IMC and how they unlock more efficient computation. We begin with a foundational overview of the field, move into the design and fabrication of computational memory devices and circuits, and close with a survey of the broader application landscape, and the interdisciplinary research directions shaping this rapidly evolving area.*

**Dr. Eunjung Cha, PSI: "High-Speed III-V Devices for Low-Noise Cryogenic Amplification"**
*The development of device technologies for low-noise amplification has historically been driven by radio astronomy and space communications, where extremely weak signals must be detected with minimal added noise. At microwave and millimeter-wave frequencies, high-speed III-V transistors have played a central role because of their high carrier mobility, excellent high-frequency performance, and ability to operate at low current levels. Cryogenic low-noise amplifiers based on these technologies are now essential for qubit readout in quantum computing. However, quantum computers capable of solving real-world problems will require large numbers of highly coherent qubits. As these systems scale, the associated readout electronics, wiring, and power consumption become major obstacles. This lecture will review the evolution of high-speed devices for cryogenic low-noise amplification, from their origins in radio astronomy and space applications to their emerging role in quantum computing. It will also discuss the current challenges and future opportunities for more scalable and energy-efficient cryogenic electronic systems.*
**Dr. Simone Iadanza, PSI: "Bypassing data transmission bottlenecks with optical Interconnects"**
*Modern datacenters and high-performance computing systems are increasingly limited by the energy and latency required to transfer the exponentially increasing data generated rather than by processing/operation performance itself. Electrical interconnects suffer from resistance, capacitance, signal loss, crosstalk and rising equalization and serialization costs. These limitations affect communication between cores, memory, chiplets, circuit boards, servers and datacenter racks. The lecture highlights how integrated photonics can pose as a solution to all these challenges, switching to optical interconnects over purely electrical wiring. Key metrics include energy per bit, bandwidth density, transmission distance, latency and total system power. The complete optical link is considered, including lasers, modulators, waveguides or fibers and photodetectors. In this lecture we will understand how silicon photonics technology, employing microcavity resonators, Mach-Zehnder modulators, wavelength-division multiplexing and optical chiplets, can be leveraged for energy efficient and ultra-fast data transfer. We will also address practical challenges such as laser efficiency, thermal control, packaging, fiber coupling and electronic interface power. We will learn to identify electrical-to-optical crossover points and evaluate optical links from a system-level perspective.*
**Prof. Adrian Ionescu,Â EPFL: "Ferro-electric devices"**
*Integrating ferroelectric properties directly into CMOS architectures, often taking the form of Negative Capacitance FETs (NC-FETs), is a major focus in microelectronics to overcome the Boltzmann thermodynamic limit of traditional transistors, whichÂ dictates that it takes at least 60 mV of gate voltage to increase the source-to-drain current by a factor of 10 at room temperature, hence Ferroelevctric FETs might be a solution for operating at vastly lower supply voltages, thereby reducving the power consumption of CMOS.*

## Note

Exam will be a multiple choice exam on the entire content of the course.

## Keywords

Nanoscale MOSFET, beyond CMOS device, energy efficient devices, ferroelectric FET, emerging memories, HEMTs, power devices, heterogeneous integration and thermal management in micorelectronics, optical interconnect.

## Learning Prerequisites

### Recommended courses

Basic engineering courses in math, solid state physics or material science

## Resources

### Moodle Link

- https://go.epfl.ch/MICRO-727